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A Low Power Self-Healing VCO Using Frequency Divider for PLL

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Abstract

The performance of the circuit may be tainted due to the outflow current and due to the changeability in the nanoscale CMOS technology. By using a frequency divider, a self-healing voltage controlled oscillator (VCO) , a broad range phase- locked loop (PLL) , and a calibrated charge pump (CP) we can put up the above issues. The PLL is fictional in a 180-nm CMOS technology. The jitter performance of the self-healing PLL will be degraded. Here the power supply consumes about 1.8 V. The simulated data presented is obtained using TANNER EDA tool with 180 nm technology. In terms of power consumption, power delay product and energy delay product, the new current comparison domino offers significant improvement compared to existing system.

Keywords- *changeability, jitter, outflow current, PLL, 180-nanometer CMOS technology***.**

1. INTRODUCTION

The circuit performances may be degraded to the non-idealities [1], [2] such as the outflow current and the changeability when the CMOS technology approaches to the nanometre scale. The large variations to degrade the device matching and performances is due to the changeability process.

This may effect in only a small number of dies on a wafer to meet the objective performance condition. The precision and resolution of analog circuits and make digital dynamic circuits not to work accurately [3], [4] due to the undesired outflow current . The source and gate of the pMOS transistor are connected to the supply voltage of 1.8 V and the transistor with W/L = 22u/7u in a 180-nm technology. The outflow current grows very quick in a high temperature atmosphere.

The phase locked loop has a wide variety of applications. PLL may be extensively employed in wire line and wire less communication systems. The divider subsequent to a VCO have to function linking the highest and lowest frequencies is used to realize wide range PLL. The deprived device matching and outflow current differ the common-mode voltage of a ring-based voltage-controlled oscillator (VCO) [5] above a broad frequency range. The oscillation frequency range of a VCO and causes a VCO not to oscillate in a most horrible case is restricted by the above issues. Dynamic circuits are essential, when the static circuits cannot function at the higher frequency where the wide range PLL mechanism. To realise a prescaler in the wide range PLL, a true-single –phase-clocking (TSPC) divider is mainly used. For a wide frequency range to cover up the process and temperature variations , a TSPC is widely used. The frequency range may be restricted by the outflow current and the original states of the floating nodes are distorted for the TSPC prescaler. The reference spur and the jitter are significantly degraded with the outflow current and the current mismatch within a calibrated charge pump.

By using the self-healing VCO and the frequency divider we know how to alleviate the above described issues. Therefore this parts are mostly used in this paper. To quantize the phase error and to digitally calibrate the charge pump a time-to-digital converter (TDC) and a 4-bit encoder is employed.

This paper is organized as follows. Section II introduces these techniques. Section III includes simulation results for the proposed circuit using TANNER EDA tool version. Section IV concludes the result.

2. CIRCUIT DESCRIPTION

2.1 PHASE-LOCKED LOOP

This Phase Locked Loop is composed of a phase-frequency detector (PFD), a digital-controlled CP, a lock detector (LD), a time-to-digital converter (TDC) [6] with a 4-bit encoder, a self-healing VCO, a frequency divider, and a second-order passive loop filter. Since the phase error of a PLL is highly dependent upon the current mismatch of a CP. The static phase error of a PFD is given as

$$\Delta\emptyset \approx \frac{\Delta i_{cp} \cdot t_{on}}{I_{CP}} \qquad (1)$$

where i_{CP} is the current difference between the pull-up and pull-down currents, I_{up} and I_{dn} , t_{on} is the turn-on

time of a PFD, I_{CP} is the averaging current of the pull-up and pull-down currents.

When this PLL locks, the LD is enabled to turn on the TDC and an encoder. A 4-bit TDC digitizes this static phase error to replicate the amount of the current mismatching. Then, the digital code of this TDC is used to calibrate the charge pump. The simulated power of this TDC is 0.24 mW. Its timing resolution is 0.3 ns and the dynamic range is 4.8 ns.

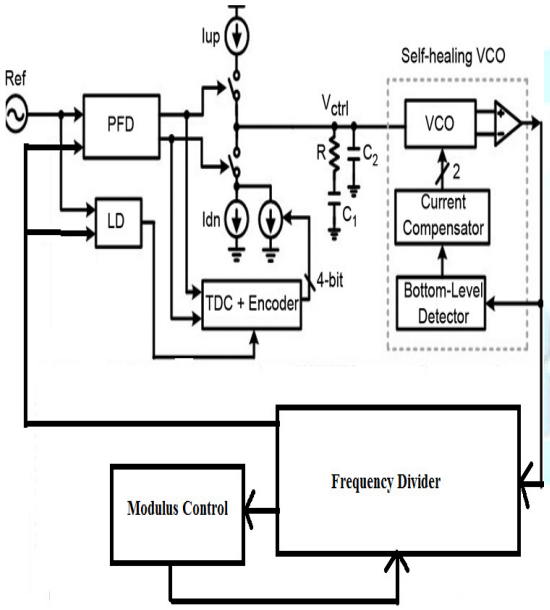

Fig. 1 Proposed PLL

2.2 SELF-HEALING VCO

A self-healing VCO is realized by four gain stages, a bottom level detector, and a current compensator. Fig. 2(a) shows a bottom-level detector, a current compensator, and a gain stage. This gain stage consists of a differential amplifier with active loads and a cross-coupled pair with digitally controlled current sources. In the differential amplifier, the transistors, M_1 and M_2 , realize the input stage, and the transistors, M_3 and M_4 , act as a variable resistor controlled by V_{ctrl}. The cross-coupled pair, M_5 and M_6 , enhances the output swing of this VCO.

The output common-mode voltage and the output swing of the VCO are distorted by the outflow currents, the total end currents, and the resistances of M_3 and M_4 . They are dependent upon the process variations. For example, when the resistances of M_3 and M_4 are decreased, the oscillation frequency of this VCO is increased. It will consequence in the output swing decreased and the bottom level is increased. It also leads to a limited oscillation frequency range. If a larger biasing current and the cross-coupled pair with larger dimensions are selected for this VCO, the output swing can be increased. However, it may waste the power when the operation frequency of this PLL is low. In this work, the self-healing VCO using a bottom-level detector can achieve a wide tuning range and low power.

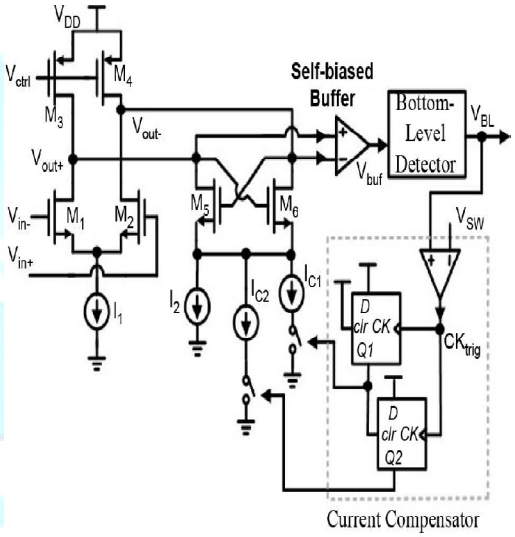

Fig. 2(a) Gain stage , a bottom level detector , and a current compensator.

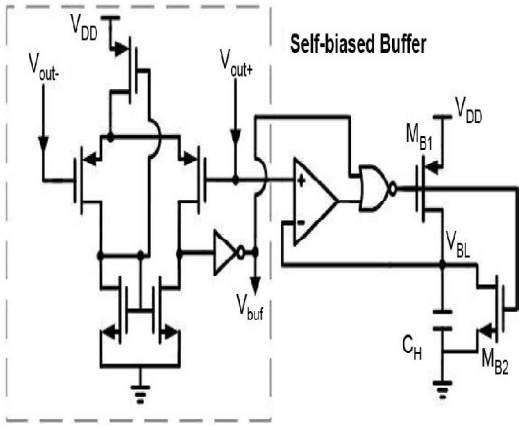

Fig. 2(b) The bottom-level detector

The bottom-level detector is shown in Fig. 2(b) and it detects the bottom level of the VCO's output swing. A self-biased buffer enlarges the output of a VCO into a rail-to-rail swing. So, the output, V_{buf}, of this self-biased

buffer and V_{out+} have the same polarity. When V_{out+} goes high and V_{buf} is high, the NOR gate will enableM_{B1} and disable M_{B2} , respectively. The current of the transistor M_{B1} will charge the capacitor, C_H, to increase V_{BL} .

When V_{out+} goes low and V_{buf} is low, two cases will be discussed. In Fig. 2(b), if the bottom level of V_{out+} is larger than V_{BL} , the comparator's output goes high and the NOR gate goes low to enable M_{B1} and disable M_{B2} , respectively. The transistor M_{B1} will charge the capacitor, C_H , to increase V_{BL} .

For the other case, if the bottom level of V_{out+} is lower than V_{BL} , the comparator's output goes low and the NOR gate goes high to disable M_{B1} and enable M_{B2} , respectively. The transistor M_{B2} will discharge the capacitor, C_H , to decrease V_{BL} . In the steady state, the voltage V_{BL} on the capacitor, C_H , will track the bottom level of the VCO's swing.

For the current compensator in Fig. 2(a), a reference voltage V_{SW} represents the target bottom level of the VCO's swing and it is compared with V_{BL} , by a comparator. When the VCO's bottom level is smaller than the target one or the output common-mode voltage of this VCO is high enough, V_{BL} is larger than V_{SW} . Then, the output of the comparator CK_{trig} goes high and enables Q1. The current compensator enables the auxiliary tail current I_{C1} to lower the output common-mode voltage.

The timing diagram is shown in Fig. 2(b). Then, it reduces the VCO's bottom level to be lower than V_{SW} . If the above case is not true, Q2 will be enabled and turn on the auxiliary tail current I_{C2} . It further lowers the VCO's bottom level.

2.3 CALIBRATED CHARGE PUMP

A 4-bit digitally-controlled CP is shown in Fig. 3 The up current has a nominal value of 200 A and the down current is digitally controlled within 180 and 210 A. The minimum current step is chosen as 2 A to relieve the worst-case current mismatch to 1% in this digitally-controlled CP. The traditional replica-biased CP needs an operational amplifier which needs a high gain and its stability must be concerned. In addition, this operational amplifier may consume a static power. The CP calibration can be finished quickly due to this digital calibration. Once the calibration is completed, the digital code is fixed and the TDC is power-downed to save a power.

2.4 FREQUENCY DIVIDER

The frequency divider is used to divide the output signal that is obtained from the self-healing VCO. A frequency divider, also called a clock divider or scaler or prescaler , is a circuit that takes an input signal of a frequency, f_{in}, and generates an output signal of a frequency:

$$f_{out} = \frac{f_{in}}{n} \qquad (2)$$

where n is an integer. Phase-locked loop frequency synthesizers make use of frequency dividers to generate a frequency that is a multiple of a reference frequency. Frequency dividers can be implemented for both analog and digital applications.

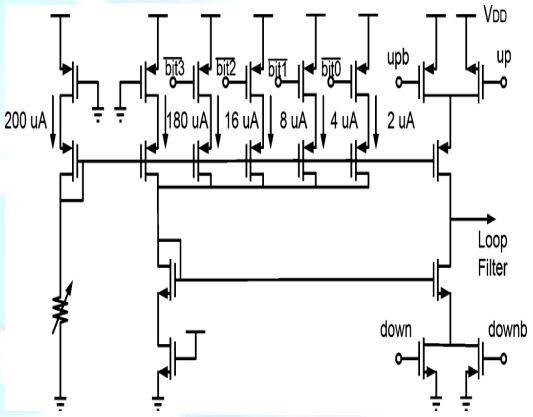

Fig. 3 A 4-bit digitally controlled charge pump

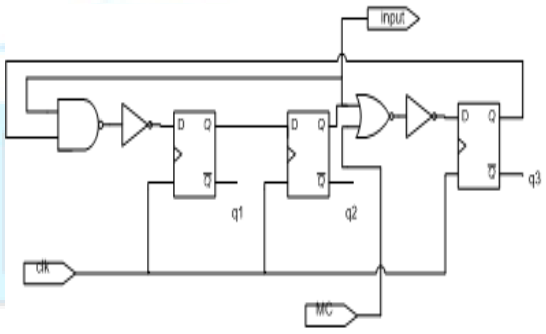

Fig. 4 Frequency divider

By using this frequency divider the area is reduced so low power consumption. Alpha latch is used to amplify the signal in order to achieve high signal strength. The speed of the PLL is increased and the delay and the power consumption reduced.

3. SIMULATION RESULTS AND COMPARISONS

The proposed circuit was simulated using Tanner EDA tool with 180nm technology. The supply voltage used in simulation is 1.8 volt. From Table 1 it is visible that average, maximum and minimum power consumption, EDP and PDP, static or dynamic current. The maximum minimum and the average power obtained for the frequency divider are 1.16 mw, 0.107 mw and 5.82 w respectively.

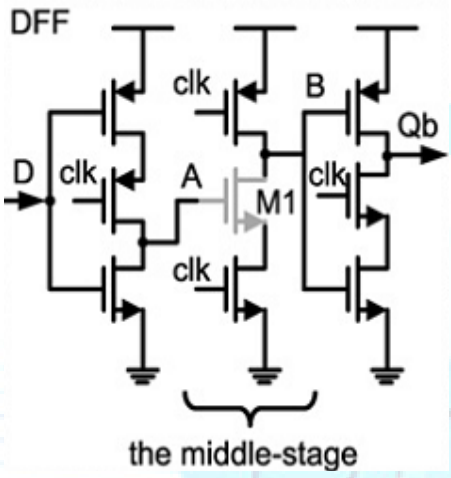

Fig. 5 D flipflop

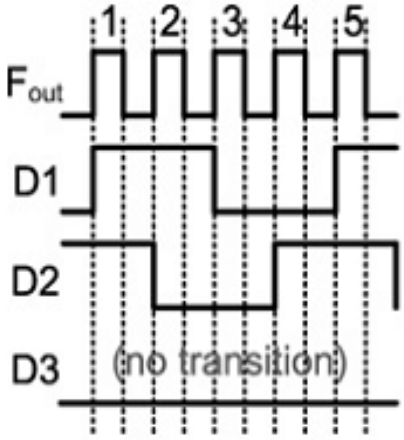

Fig. 6 D flipflop wave form

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TABLE 1

Comparison of different parameters in PLL

Parameter	Self-healing VCO	Frequency divider
Power	1.95 kw	5.82 w
Maximum power	2.29 mw	1.16mw
Minimum power	40.47mw	0.107 mw
PDP	45.88nw/s	23.2nw/s
EDP	91.77pw/s	0.464pw/s
Static or dynamic current	1.27 mA	0.64 mA
Area of transistors	2772um^2	1012um^2

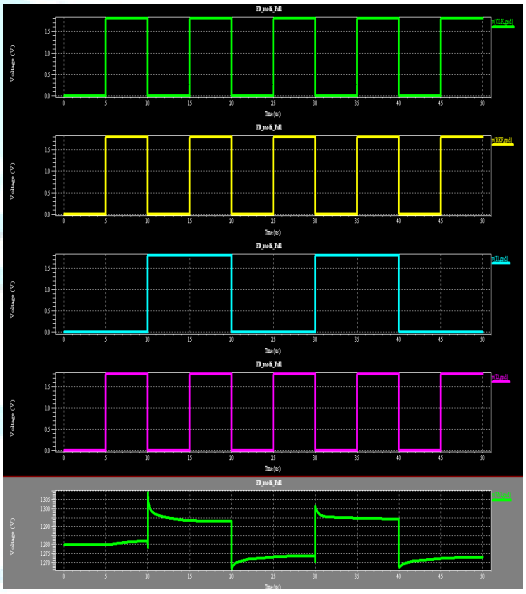

Fig. 7 Simulated waveform of the proposed PLL

4. CONCLUSION

The wide range PLL using frequency divider is fabricated in 180-nm CMOS process. To deal with the outflow current and the changeability process in the nanoscale CMOS process, a self-healing VCO, calibrated charge pump and a frequency divider are used which will reduce the power, delay and area. And it will increase the signal strength and speed.

REFERENCES

[1] L. L. Lewyn, T. Ytterdal, C. Wulff, and K. Martin, "Analog circuit design in nanoscale CMOS technologies," *Proc. IEEE*, vol. 18, no. 11, pp. 1687–1714, Oct. 2009.

[2] J.M.Wang, Y. Cao, M. Chen, J. Sun, and A. Mitev, "Capturing device mismatch in analog and mixed-signal designs," *IEEE Circuits Syst. Mag.*, vol. 8, no. 4, pp. 137–144, Dec. 2008.

[3] K. Agawa, H. Hara, T. Takayanagi, and T. Kuroda, "A bitline leakage compensation scheme for low-voltage SRAMs," *IEEE J. Solid-State Circuits*, vol. 36, no. 5, pp. 726–734, May 2001.

[4] R. Krishnamurthy, A. Alvandpour, G. Balamurugan, N. Shanbhag, K. Soumyanath, and S. Borkar, "A 130-nm 6-GHz256 32b leakage-tolerant register file," *IEEE J. Solid-State Circuits*, vol. 37, no. 5, pp. 624–632, May 2002.

[5] R. Holzer, "A 1 V CMOS PLL designed in high-leakage CMOS process operating at 10–700 MHz," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2002, pp. 272–273..

[6] P. Dudek, S. Szczepanski, and J. Hatfield, "A high-resolution CMOS time-to-digital converter utilizing a vernier delay line," *IEEE J. Solid- State Circuits*, vol. 35, no. 2, pp. 240–247, Feb. 2000

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